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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,810	10/30/2003	Jung-Fang Chang	CHAN3225/EM	6888

23364 7590 08/24/2005

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EXAMINER	
SANEI, HANA ASMAT	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/695,810	CHANG ET AL.	
	Examiner	Art Unit	
	Hana A. Sanei	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of a certified copy of the #092123813 application referred to in the oath or declaration or in an application data sheet. If this copy is being filed to obtain the benefits of the foreign filing date under 35 U.S.C. 119(a)-(d), applicant should also file a claim for such priority as required by 35 U.S.C. 119(b). If the application being examined is an original application filed under 35 U.S.C. 111(a) (other than a design application) on or after November 29, 2000, the claim for priority must be presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. See 37 CFR 1.55(a)(1)(i). If the application being examined has entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and Regulations of the PCT. See 37 CFR 1.55(a)(1)(ii). Any claim for priority under 35 U.S.C. 119(a)-(d) or (f) or 365(a) or (b) not presented within the time period set forth in 37 CFR 1.55(a)(1) is considered to have been waived. If a claim for foreign priority is presented after the time period set forth in 37 CFR 1.55(a)(1), the claim may be accepted if the claim properly identifies the prior foreign application and is accompanied by a grantable petition to accept an unintentionally delayed claim for priority. See 37 CFR 1.55(c).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,3-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya (US 6814832) in view of Leib et al. (US 2004/0214380 A1).

With respect to Claim 1, Utsunomiya discloses a method for manufacturing a flexible panel comprising (Figure 1D-1E): (a) providing a first substrate (insulation layer, 31) having a plurality of functional switches or conducting lines (TFT, 3) thereon; (b) bonding a second substrate on said plurality of functional switches or conducting lines (temporary transfer substrate, 5); (e) removing said second substrate (Fig. 1E).

Utsunomiya is silent regarding a thinning of the first substrate. In the same field of endeavor, Leib discloses the thinning (Figure 2A-2C) of said first substrate (6) to a predetermined thickness in order to allow for the conductive material to be within a closer proximity to the flexible substrate that will be added in a following step. It should be noted that the minimal thickness in the first substrate (Fig. 1D, 31) of Utsunomiya is essential in order to allow the TFT (3) to be electrically connected to a flexible third substrate (6). Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to add the step of thinning of the first substrate, as disclosed by Leib, in the panel of Utsunomiya. Motivation to combine would be to allow for the

conductive material to be within a closer proximity to the flexible substrate that will be added in a following step.

Utsunomiya is further silent regarding the adhering or sealing of a flexible third substrate onto the first substrate. In the same field of endeavor, Leib discloses the adhering or sealing a flexible third substrate (encapsulation, 25) on said first substrate, wherein said first substrate is sandwiched between said second substrate and said third substrate (Fig. 2C) in order to preserve the mechanical strength while maintaining product weight at a minimum. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to add the flexible substrate, as disclosed by Leib, in the panel of Utsunomiya. Motivation to combine would be to preserve the mechanical strength while maintaining product weight at a minimum.

With respect to Claim 3, Utsunomiya discloses that the first substrate is a glass substrate (Col. 9, lines 51-55).

With respect to Claim 4, Utsunomiya is silent regarding a thinning method of the first substrate that is polishing. In the same field of endeavor, Leib discloses a thinning method of the first substrate that is polishing (grounding, Page 4, Paragraph [0055]) in order to allow for the conductive material to be within a closer proximity to the flexible substrate that will be added in a following step. Examiner notes that polishing is a *rubbing* process and furthermore, grounding may be completed by the *rubbing* of two hard surfaces. It should be noted that the minimal thickness in the first substrate (Fig. 1D, 31) of Utsunomiya is essential in order to allow the TFT (3) electrically connected to a flexible third substrate (6). Therefore, it would have been obvious to one of ordinary

skill in the art, at the time of the invention, to add the step of thinning of the first substrate, as disclosed by Leib, in the panel of Utsunomiya. Motivation to combine would be to allow for the conductive material to be within a closer proximity to the flexible substrate that will be added in a following step.

With respect to Claim 5, Utsunomiya discloses that the switch is a thin film transistor (Col. 7, lines 47-50).

With respect to Claim 7, Utsunomiya discloses that the flexible third substrate is made of plastic (Col. 13, lines 11-16).

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya (US 6814832) in view of Leib et al. (US 2004/0214380 A1) with further consideration to Gourlay (US 2004/0097161 A1).

With respect to Claim 2, Utsunomiya-Leib discloses the embodiment described above (see Claim 1 rejection above) and further includes step (f) of forming a plurality of light valves, light-emitters, or conducting layers on said plurality of switches or conducting lines (Col. 3, lines 31-43).

Utsunomiya-Leib is silent regarding the adhering or sealing of a flexible fourth substrate on said plurality of light valves, light-emitters, or conducting layers after said step (e), wherein said plurality of light valves, light-emitters, or conducting layers are located between said third substrate and said fourth substrate. In the same field of endeavor, Gourlay discloses the adhering or sealing of a flexible fourth substrate (Page 2, Paragraph [0025], Figure 2, #15) on said plurality of light valves, light-emitters, or conducting layers (active electronic circuitry, 14) after said step (e), wherein said

plurality of light valves, light-emitters, or conducting layers are located between said third substrate and said fourth substrate (Fig. 2) in order to add further flexibility while maintaining the mechanical stability. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to add the step a flexible fourth substrate on said plurality of light valves, light-emitters, or conducting layers after said step (e), as disclosed by Gourlay, in the panel of Utsunomiya-Leib. Motivation to combine would be to add further flexibility while maintaining the mechanical stability.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya (US 6814832) in view of Leib et al. (US 2004/0214380 A1) with further consideration to Young (US 2002/0139981 A1).

With respect to Claim 6, Utsunomiya-Leib is silent regarding the thickness range of the thinned first substrate. In the same field of endeavor, Young teaches that the first substrate is thinned to have a thickness ranging from 30 to 100.mu.m (Page 4, Paragraph [0042]) in order to allow the matrix circuit to be electrically connected to a flexible third substrate, which would be added in a following step. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the thickness of a first substrate, as disclosed by Young, in the panel of Utsunomiya-Leib. Motivation to combine would be to allow the matrix circuit to be electrically connected to a flexible third substrate, in which the flexible third substrate would be added in a following step.

4. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya (US 6814832) in view of Leib et al. (US 2004/0214380 A1) in view of Gourlay (US 2004/0097161 A1) with further consideration to Hishida (US 6861802 B2).

With respect to Claim 8, Utsunomiya-Leib-Goulay teaches the invention set forth above (see rejection in Claim 2 above). Utsunomiya-Leib-Goulay is silent regarding bonding a fourth substrate on said thinned first substrate. In the same field of endeavor, Hishida teaches bonding a flexible fourth substrate on said thinned first substrate (Col. 4, lines 21-27), wherein said first substrate, said plurality of light valves, light-emitters, or conducting layers, and said plurality of functional switches or conducting lines are located between said third substrate and said fourth substrate (Col. 4, lines 21-27) in order to add further flexibility while maintaining the mechanical stability. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to add the flexible fourth substrate on said thinned first substrate, as disclosed by Hishida, in the panel of Utsunomiya-Leib-Goulay. Motivation to combine would be add further flexibility while maintaining the mechanical stability

With respect to Claim 9, Utsunomiya discloses that the first substrate is a glass substrate (Col. 9, lines 51-55).

With respect to Claim 10, Leib discloses a thinning method of the first substrate that is polishing (grounding, Page 4, Paragraph [0055]). Examiner notes that polishing is a *rubbing* process and furthermore, grounding may be completed by the *rubbing* of two hard surfaces.

With respect to Claim 11, Utsunomiya discloses that the switch is a thin film transistor (Col. 7, lines 47-50).

With respect to Claim 13, Utsunomiya discloses that the flexible third substrate is made of plastic (Col. 13, lines 11-16).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya (US 6814832) in view of Leib et al. (US 2004/0214380 A1) in view of Hishida (US 6861802 B2) with further consideration to Young (US 2002/0139981 A1).

With respect to Claim 12, Utsunomiya-Leib-Hishida is silent regarding the thickness range of the thinned first substrate. In the same field of endeavor, Young teaches that the first substrate is thinned to have a thickness ranging from 30 to 100.mu.m (Page 4, Paragraph [0042]) in order to allow the matrix circuit to be electrically connected to a flexible third substrate, which would be added in a following step. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the thickness of a first substrate, as disclosed by Young, in the panel of Utsunomiya-Leib-Hishida. Motivation to combine would be to allow the matrix circuit to be electrically connected to a flexible third substrate, in which the flexible third substrate would be added in a following step.

Allowable Subject Matter

Claims 14-20 are allowed over the prior art of record.

The following is an examiner's statement of reason for allowance:

Regarding Claim 14, the prior art of record neither shows nor suggests a method for manufacturing a flexible panel comprising all of the limitation set forth in Claim 14, particularly comprising the limitations of removing the fifth substrate on said first substrate, together with the other cited limitations.

Claims 15-20 are allowable for their dependency upon an allowable claim.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Jindai et al. (US 6824437)

Tsutsui et al. (US 6824437)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hana A. Sanei whose telephone number is (571) 272-8654. The examiner can normally be reached on Monday- Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner,
Hana Sanei

Karabi Guharay
KARABI GUHARAY
PRIMARY EXAMINER